Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process for estimating power consumption, over a given time interval, of a digital circuit described at a hardware level ~~of a simulated~~ using a functional element provided with input/output terminals, the process comprising:

estimating the power consumption based on a number of transitions performed by the ~~simulated~~ functional element during said time interval, including:

emulating, at ~~a~~ said hardware level, ~~corresponding to an abstraction level of~~ the digital circuit, using additional elements associated to and coupled to said functional element at said hardware level, said additional ~~emulated~~ elements being able to detect, during emulation of the digital circuit, at least one signal indicative of a behavior, and hence of power consumption, of the associated functional element ~~associated~~ during said time interval; and

acquiring a value of said at least one signal during the emulation of the digital circuit, said value being indicative of the number of transitions and usable to determine the power consumption of said associated functional element in said given time interval.

2. (Currently Amended) The process according to claim 1 wherein emulating said digital circuit using said additional elements ~~are emulated by associating them~~ associated to and coupled to said functional element includes coupling said additional elements to an output of the functional element.

3. (Currently Amended) The process according to claim 1 wherein said additional ~~emulated~~ elements are able to ~~detect~~obtain, during said given time interval and during said emulation of the digital circuit:

a count of said transitions to obtain said number of transitions,

a fraction of time in which a state of the associated functional element is stable, and

the value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval.

4. (Previously Presented) The process according to claim 1, further comprising controlling acquisition of the value of said at least one signal using hardware events monitored by logic analyzers active on the additional elements.

5. (Currently Amended) The process according to claim 1, further comprising accessing information stored in said additional ~~emulated~~ elements and storing said information in view of a subsequent processing.

6. (Previously Presented) A processing system configured to implement the process according to claim 1.

7. (Previously Presented) A computer program product directly loadable into an internal memory of a digital computer, comprising software code portions to perform the process of claim 1 when said product is run on the computer.

8. (Previously Presented) The process of claim 1 wherein emulating at the hardware level includes emulating at a register transfer level (RTL).

9. (Previously Presented) The process of claim 1 wherein emulating at the hardware level includes emulating at a gate level.

10. (Currently Amended) A system for estimating power consumption, over a given time interval, of a digital circuit described at a hardware level ~~of a simulated~~using a functional element provided with input/output terminals, the ~~process~~ system comprising:

means for emulating, at ~~a~~ said hardware ~~abstraction~~ level, ~~corresponding to an abstraction level of~~ the digital circuit~~,~~ using an additional element associated to and coupled to the functional element at said hardware level, the additional ~~emulated~~ element being able to detect, during emulation of the digital circuit, at least one signal indicative of a behavior of the associated functional element ~~associated~~ during the time interval; ~~and~~

means for acquiring a value of the at least one signal, the value being acquired during the emulation of the digital circuit and being indicative of the number of transitions performed by the ~~simulated~~ functional element during the time interval; and

means for estimating the power consumption based on the acquired number of transitions performed by the ~~simulated~~ functional element during the time interval.

11. (Previously Presented) The system of claim 10 wherein the additional element is able to detect, during the given time interval, a fraction of time in which a state of the associated functional element is stable, the means for estimating using the value of the number of transitions and the fraction of time to determine the power consumption of the functional element during the time interval.

12. (Currently Amended) The system of claim 10 wherein the hardware ~~abstraction~~ level is an RTL level or a gate level.

13. (Currently Amended) An apparatus to estimate power consumption, over a given time interval, of a digital circuit described at a hardware level ~~of a simulated~~using a functional element provided with input/output terminals, the apparatus ~~including~~ comprising:

a first module to emulate, at ~~a~~ said hardware ~~abstraction~~ level, ~~corresponding to an abstraction level of~~ the digital circuit~~,~~ using an additional element associated to and coupled to the functional element at said hardware level, the additional ~~emulated~~ element being able to

detect, during emulation of the digital circuit, at least one signal indicative of a behavior of the associated functional element ~~associated~~ during the time interval;

a second module operatively coupled to the first module to acquire a value of the at least one signal, the value being acquired during the emulation of the digital circuit and being indicative of the number of transitions performed by the ~~simulated~~ functional element during the time interval; and

a third module operatively coupled to the second module to estimate the power consumption based on the acquired number of transitions performed by the ~~simulated~~ functional element during the time interval.

14. (Previously Presented) The apparatus of claim 13 wherein the additional element is able to detect, during the given time interval, a fraction of time in which a state of the associated functional element is stable, the third module being operative to use the value of the number of transitions and the fraction of time to determine the power consumption of the functional element during the time interval.

15. (Previously Presented) The apparatus of claim 13 wherein the third module includes machine-readable instructions stored on a machine-readable medium and executable by a processor.

16. (Currently Amended) The apparatus of claim 13 wherein the wherein the hardware ~~abstraction~~ level is an RTL level or a gate level.

17. (New) The method of claim 1 wherein using said additional elements coupled to said functional element at said hardware level includes:

modifying said digital circuit at said hardware level by adding at least one of said additional elements to said functional element to allow said added additional element to form part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit.

18. (New) The method of claim 1 wherein using said additional elements to detect said at least one signal during said emulation of the digital circuit includes:

detecting, during operation of said digital circuit, said number of transitions.

19. (New) The method of claim 1 wherein acquiring said value indicative of the number of transitions to determine the power consumption includes acquiring said value in real time.

20. (New) The system of claim 10 wherein said additional element, coupled to said functional element at said hardware level, modifies said digital circuit at said hardware level by forming part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit.

21. (New) The system of claim 10 wherein said additional element to detect said at least one signal during said emulation of the digital circuit includes:

means for detecting, during operation of said digital circuit, said number of transitions.

22. (New) The apparatus of claim 13 wherein said additional element, coupled to said functional element at said hardware level, modifies said digital circuit at said hardware level by forming part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit.

23. (New) The apparatus of claim 13 wherein said additional element is adapted to detect, during operation of said digital circuit, said number of transitions.